Claims

What is claimed is:

1. A charge pump for a phase-locked loop circuit suitable for use in a mixed signal integrated circuit, the charge pump having complementary P- and N-channel charge pump devices, comprising:

a constant current generator suitable for generating a current reference for providing a substantially constant gate-to-source bias for the P- and N-channel charge pump devices;

a differential pair of P-channel pass-gate devices suitable for isolating the P-channel charge pump device from supply and ground transients in the mixed signal integrated circuit; and

a differential pair of N-channel pass-gate device suitable for isolating the N-channel charge pump device from supply and ground transients in the mixed signal integrated circuit

wherein the charge pump is capable of substantially eliminating loss of lock by the phase-locked loop circuit due to supply and ground transients.

2. The charge pump as claimed in claim 1, wherein the current reference generated by the constant current generator comprises a high power supply rejection for the P- and N- channel charge pump devices.

3. The charge pump as claimed in claim 1, wherein the constant current generator comprises P- and N- channel bias devices, and wherein the P- and N- channel charge pump devices function as current mirrors of the P- and N-channel bias devices.

4. The charge pump as claimed in claim 3, wherein the P- and N- channel charge pump devices have a substantially constant current.

5. The charge pump as claimed in claim 1, wherein the phase-locked loop circuit includes a phase detector having P- and N- channel drivers, and wherein the P- and N-channel pass gate devices have an on/off state, and wherein the on/off state of the P- and N-channel pass-gate devices is controlled in accordance with the P- and N-channel drivers.

6. The charge pump as claimed in claim 1, wherein the P- and N- channel phase gate devices comprise an on-resistance, and wherein the supply and ground transients are restricted to the P- and N-channel pass-gate devices' on-resistance.

7. The charge pump as claimed in claim 1, wherein the constant current source is programmable.

8. A phase-locked loop circuit suitable for use in a mixed signal integrated circuit, comprising:

a phase detector; and

a charge pump driven by the phase detector, the charge pump having complementary P- and N-channel charge pump devices, the charge pump including:

a constant current generator suitable for generating a current reference for providing a substantially constant gate-to-source bias for the P- and N-channel charge pump devices;

a first differential pair of pass-gate devices suitable for isolating the P-channel charge pump device from supply and ground transients in the mixed signal integrated circuit; and

a second differential pair of pass-gate devices suitable for isolating the N-channel device from supply and ground transients in the mixed signal integrated circuit.

9. The phase-locked loop circuit as claimed in claim 8, wherein the current reference generated by the constant current generator comprises a high power supply rejection for the P- and N- channel charge pump devices.

10. The phase-locked loop circuit as claimed in claim 8, wherein the constant current generator comprises P- and N- channel bias devices, and wherein the P- and N-channel charge pump devices function as current mirrors of the P- and N-channel bias devices.

11. The phase-locked loop circuit as claimed in claim 10, wherein the P- and N-channel charge pump devices have a substantially constant current.

12. The phase-locked loop circuit as claimed in claim 8, wherein the phase detector comprises P- and N- channel drivers, and wherein the P- and N- channel pass gate

devices have an on/off state, and wherein the on/off state of the P- and N-channel pass-gate devices is controlled in accordance with the P- and N-channel drivers.

13. The phase-locked loop circuit as claimed in claim 8, wherein the P- and N-channel phase gate devices comprise an on-resistance, and wherein the supply and ground transients are restricted to the P- and N-channel pass-gate devices' on-resistance.

14. The phase-locked loop circuit as claimed in claim 8, wherein the charge pump is programmable.

15. A mixed signal integrated circuit having a phase-locked loop circuit, comprising:

a phase detector; and

a charge pump driven by the phase detector, the charge pump having complementary P- and N-channel charge pump devices, the charge pump including:

a constant current generator suitable for generating a current reference for providing a substantially constant gate-to-source bias for the P- and N-channel charge pump devices;

a first differential pair of pass-gate devices suitable for isolating the P-channel charge pump device from supply and ground transients in the mixed signal integrated circuit; and

a second differential pair of pass-gate devices suitable for isolating the N-channel device from supply and ground transients in the mixed signal integrated circuit.

16. The mixed signal integrated circuit as claimed in claim 15, wherein the current reference generated by the constant current generator comprises a high power supply rejection for the P- and N- channel charge pump devices.

17. The mixed signal integrated circuit as claimed in claim 15, wherein the constant current generator comprises P- and N- channel bias devices, and wherein the P- and N- channel charge pump devices function as current mirrors of the P- and N-channel bias devices.

18. The mixed signal integrated circuit as claimed in claim 17, wherein the P- and N- channel charge pump devices have a substantially constant current.

19. The mixed signal integrated circuit as claimed in claim 15, wherein the phase detector comprises P- and N- channel drivers, and wherein the P- and N- channel pass gate

devices have an on/off state, and wherein the on/off state of the P- and N-channel pass-gate devices is controlled in accordance with the P- and N-channel drivers.

20. The mixed signal integrated circuit as claimed in claim 15, wherein the P- and N- channel phase gate devices comprise an on-resistance, and wherein the supply and ground transients are restricted to the P- and N-channel pass-gate devices' on-resistance.

21. The mixed signal integrated circuit as claimed in claim 15, wherein the charge pump is programmable.